Amendments to the Specification:

Please amend the paragraph beginning on Page 6, line 21 as follows:

Referring to FIG. 4A, a transistor according to some embodiments of the invention includes a fin 56 that is a vertically protruding portion of semiconductor substrate. A buffer oxide layer 58 is formed on the substrate. The buffer oxide layer 58 is formed on the lower sidewalls of the fin 56, and a gate insulating layer 64 is formed on the upper sidewalls of the fin 56. The buffer oxide layer 58 and the gate insulating layer 64 form a boundary at a height above the substrate 50. The fin 56 may be formed 50-1000nm in height, and the buffer oxide layer 58 may be formed about 2-50nm in height. The gate insulating layer 64 may be formed of thermal oxide, CVD oxide, or nitride. The thickness and material of the layer can be selected according to the characteristic needs of the devices. A nitride liner 60a is formed on the buffer oxide layer 58, neighboring the lower sidewall of the fin 56 and extending on the sidewall away from the substrate 50 to beyond the gate insulating layer 64. A device isolation layer 62a is formed adjacent to the fin 56, and is separated from the fin 56 by the nitride liner 60a. The device isolation layer 62a is formed to define recesses on both sides of the fin 56. The nitride liner 60a may be formed to thickness of 5-200nm. The height of the fin 56 which protrudes over the nitride liner 60a defines the channel width of the transistor. The fin 56 may be formed to thickness of about 10-500nm. A gate electrode 66 crosses over (i.e. is positioned on) the fin 56. The gate electrode 66 may be a stacked structure of low resistance conductive layers 66b, such as metal, metallic silicide, and polysilicon or polysilicon germanium (SiGe). As illustrated in FIG. 4A, the top surfaces of the fin 56 and the device isolation layer 62a may be of similar height or different in height. In some embodiments according to the invention, the top edges of the fin 56 are rounded . The portion of the fin 56 protruding from the nitride liner 60a is surrounded by the gate electrode 66, defining the channel width of the transistor. In addition, the top surface of the gate electrode 66 may be planar, because of the ratio of the entire device region to the region between the fin 56 and the device isolation layer 62a. Although not shown in the drawing, impurities may be implanted into the fin 56 at both sides of the gate electrode 66 to form the source and drain regions of the transistor. A channel region may be formed in the fin 56 with or without

implanted impurities. In some embodiments, the gate electrode 66 extends toward the substrate 50 to beyond the junction boundaries of the source and drain regions (illustrated by the dashed line), to reduce the likelihood of parasitic transistor formation.